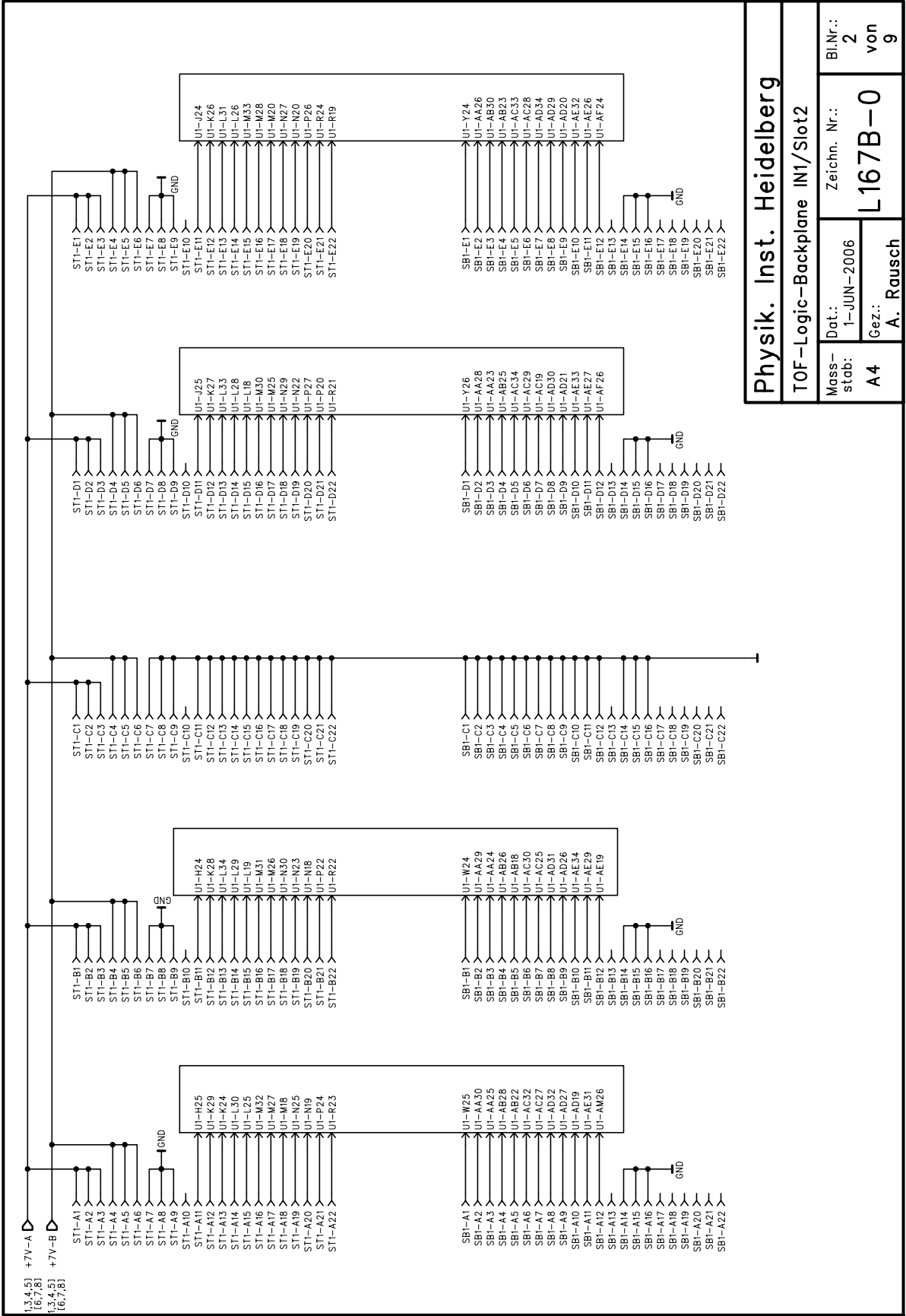
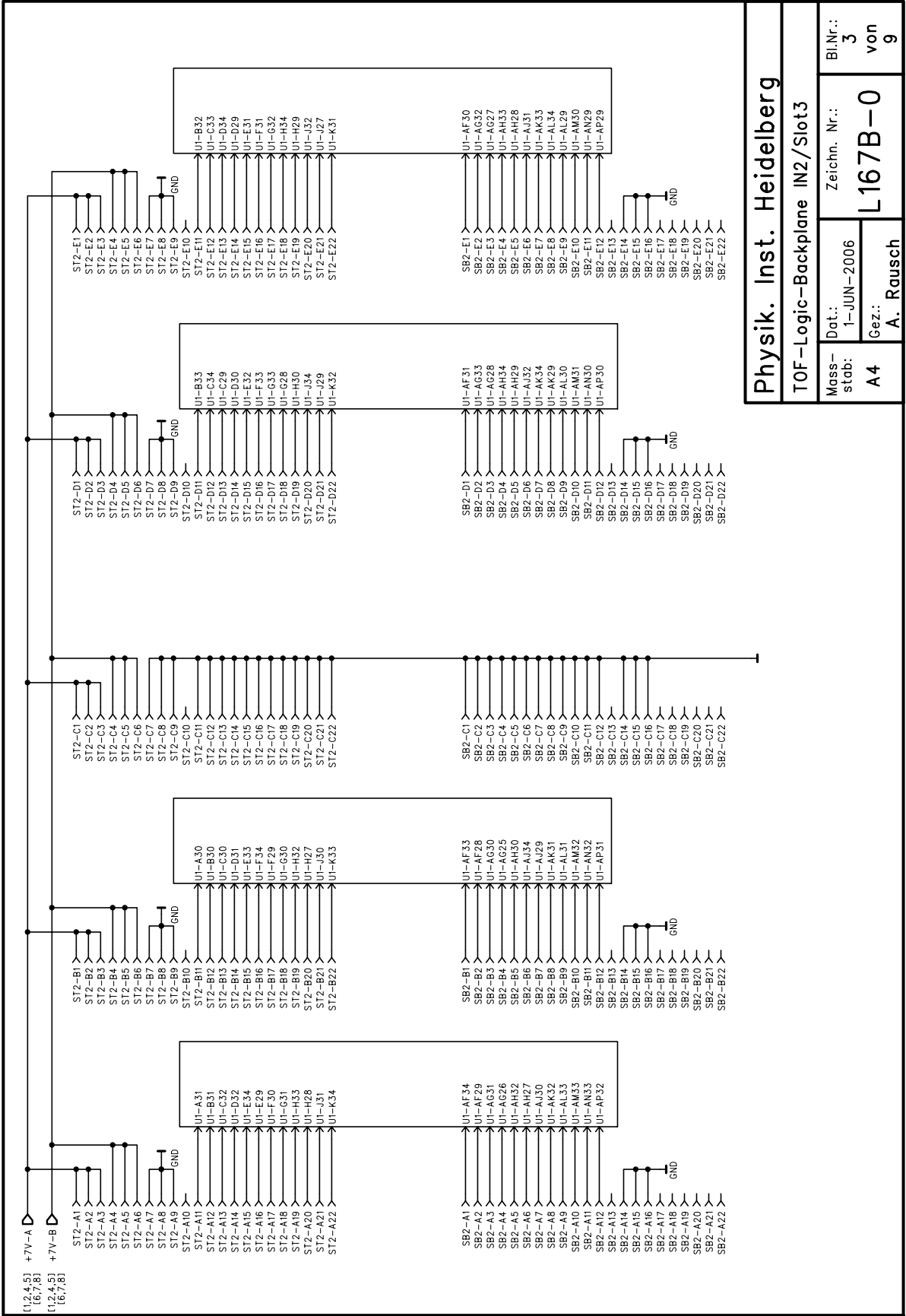


<b>Physik. Inst. Heidelberg</b>	
<b>TOF-Logic-Backplane Power/Slot1</b>	
Massstab: A4	Zeichn. Nr.: L167B-0
Dat.: 1-JUN-2006	Bl.Nr.: 1 von 9
Gez.: A. Rausch	

- M1 ●
- M2 ●
- M3 ●
- M4 ●
- M5 ●
- M6 ●
- M7 ●
- M8 ●
- M9 ●
- M10 ●
- M11 ●
- M12 ●
- M13 ●
- M14 ●
- M15 ●
- M16 ●
- M17 ●
- M18 ●
- M19 ●
- M20 ●
- K1 ●
- K2 ●
- K3 ●
- K4 ●
- Y1 ●
- Y2 ●
- Y3 ●
- Y4 ●



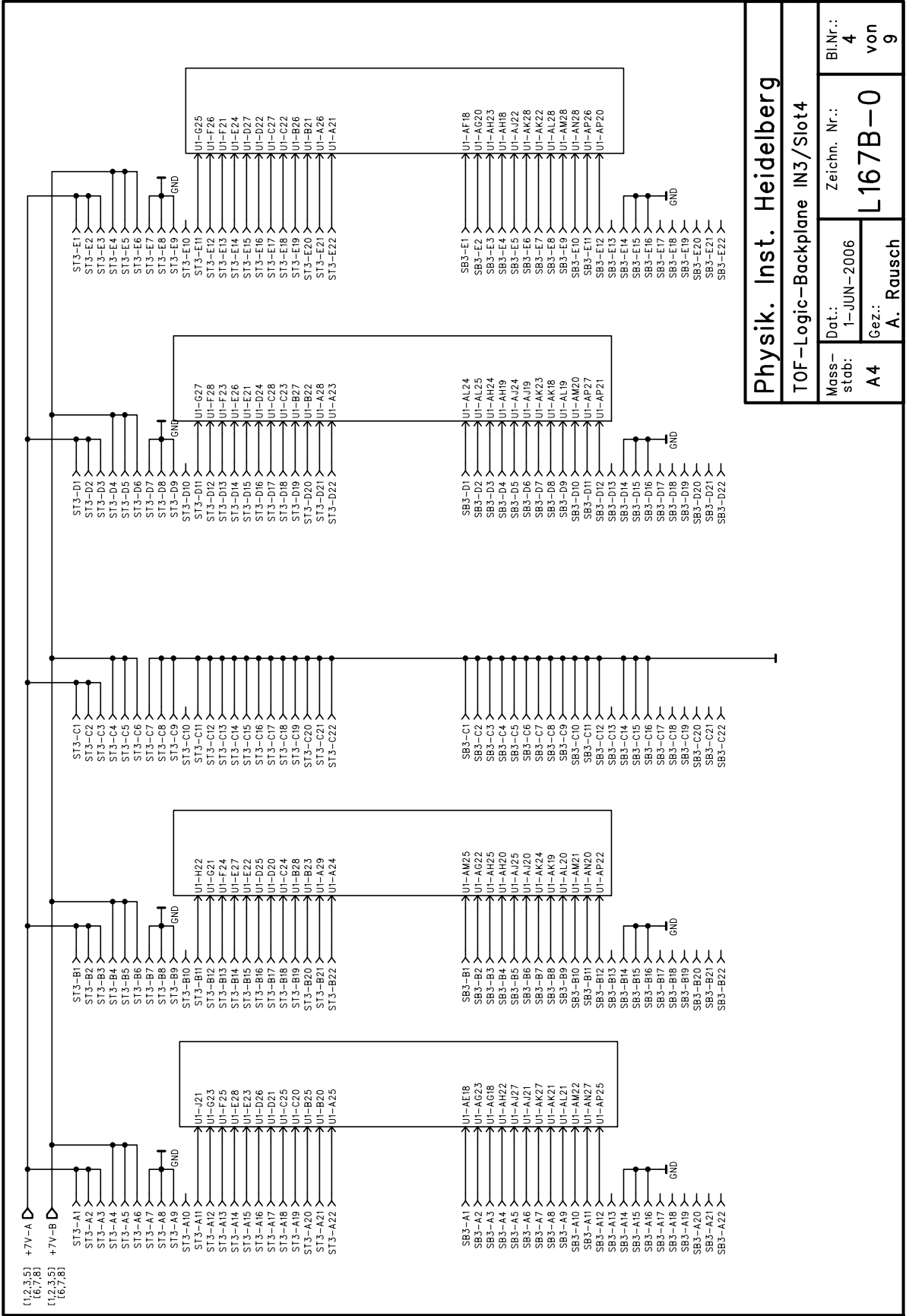
<b>Physik. Inst. Heidelberg</b> TOF-Logic-Backplane IN1/Slot2		Zeichn. Nr.: <b>L167B-0</b>	Bl.Nr.: <b>2</b> von <b>9</b>
		Mass- stab: <b>A4</b>	Dat.: 1-JUN-2006 Gez.: <b>A. Rausch</b>



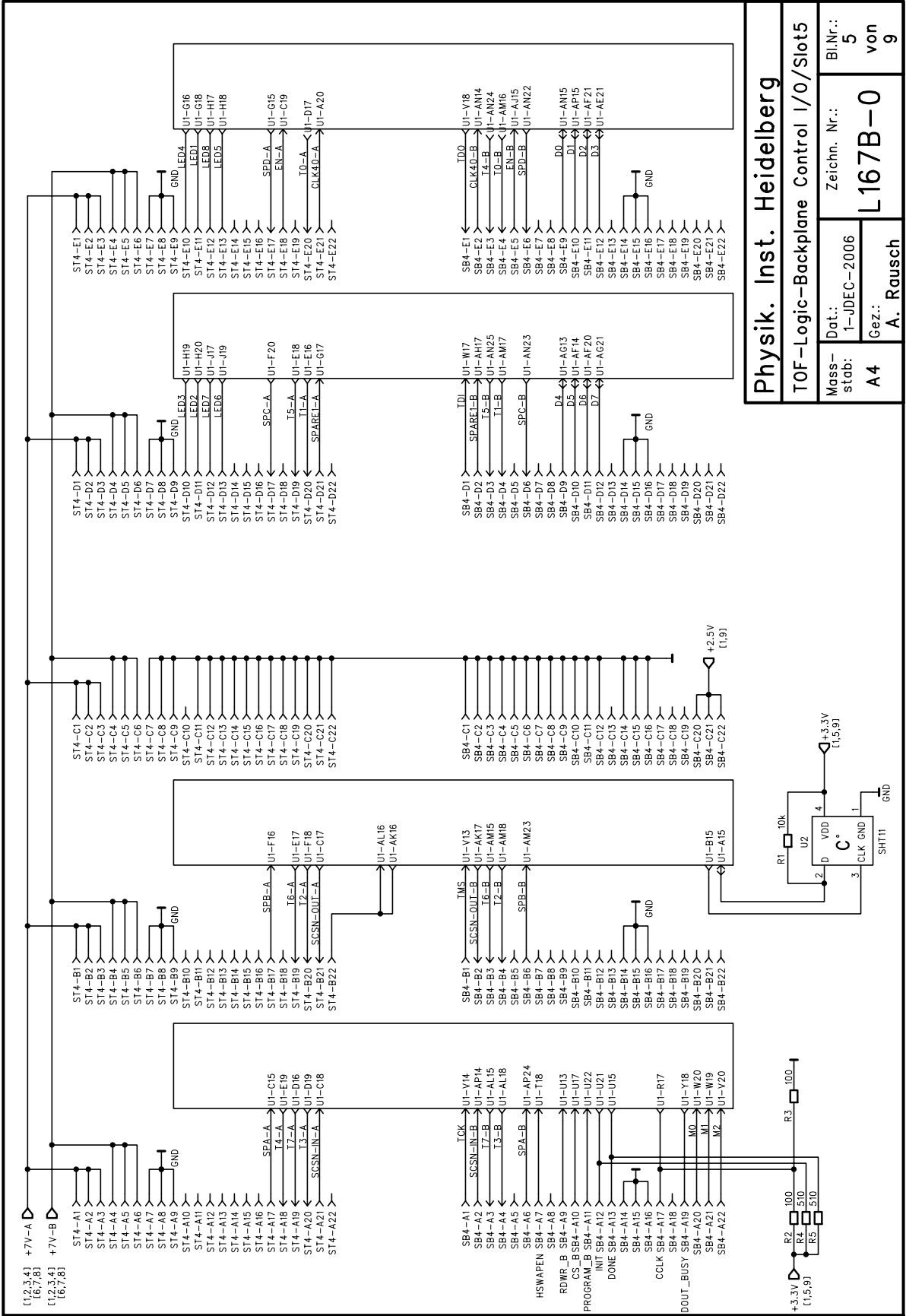
# Physik. Inst. Heidelberg

TOF-Logic-Backplane IN2/Slot3

Massstab:	A4	Zeichn. Nr.:	L167B-0	Bl.Nr.:	3
Dat.:	1-JUN-2006	Gez.:	A. Rausch	von	9



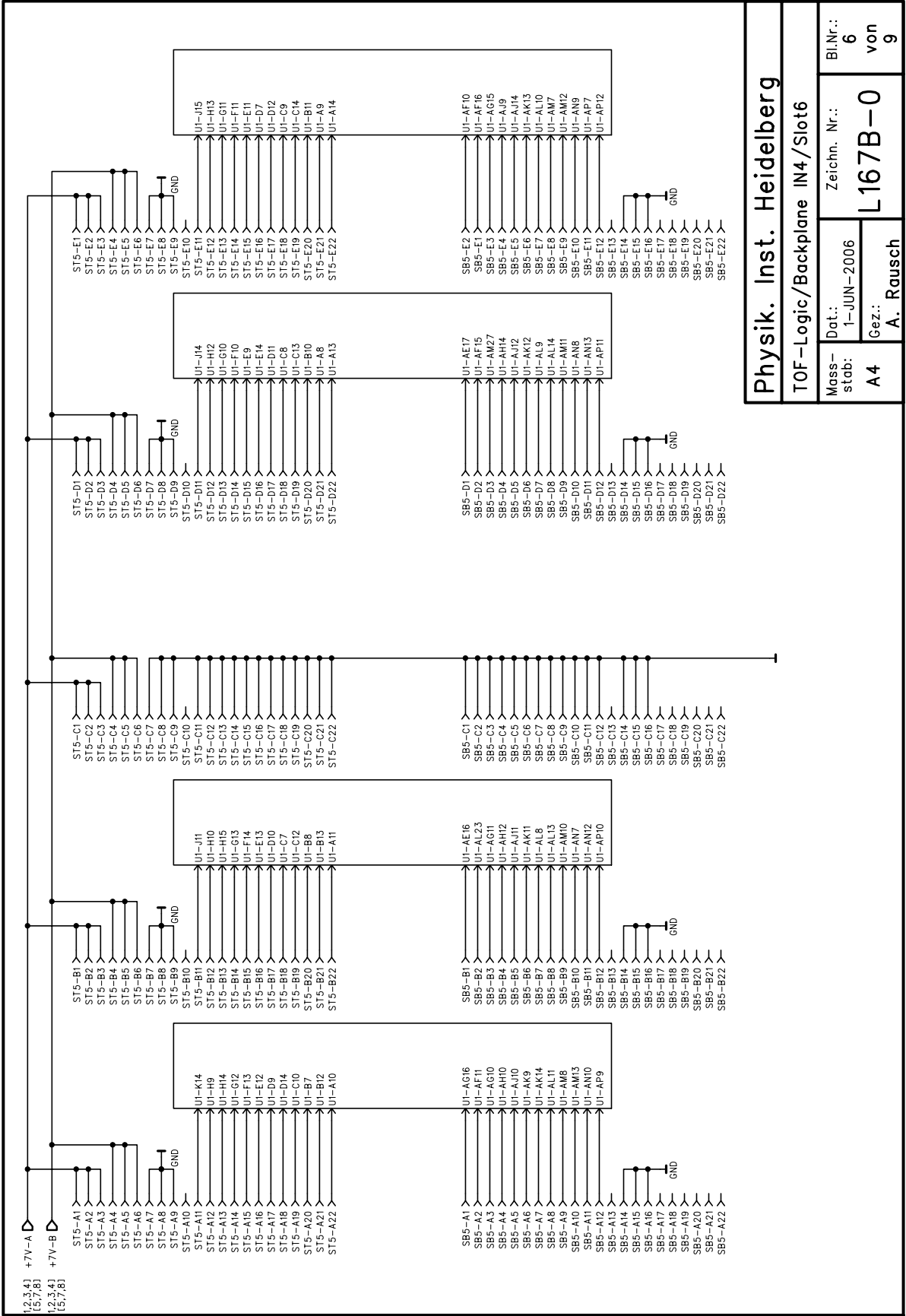
Physik. Inst. Heidelberg		TOF-Logic-Backplane IN3/Slot4	
		Massstab: A4	Dat.: 1-JUN-2006
Bl.Nr.: 4 von 9		Zeichn. Nr.: L167B-0	
		Gez.: A. Rausch	



**Physik. Inst. Heidelberg**

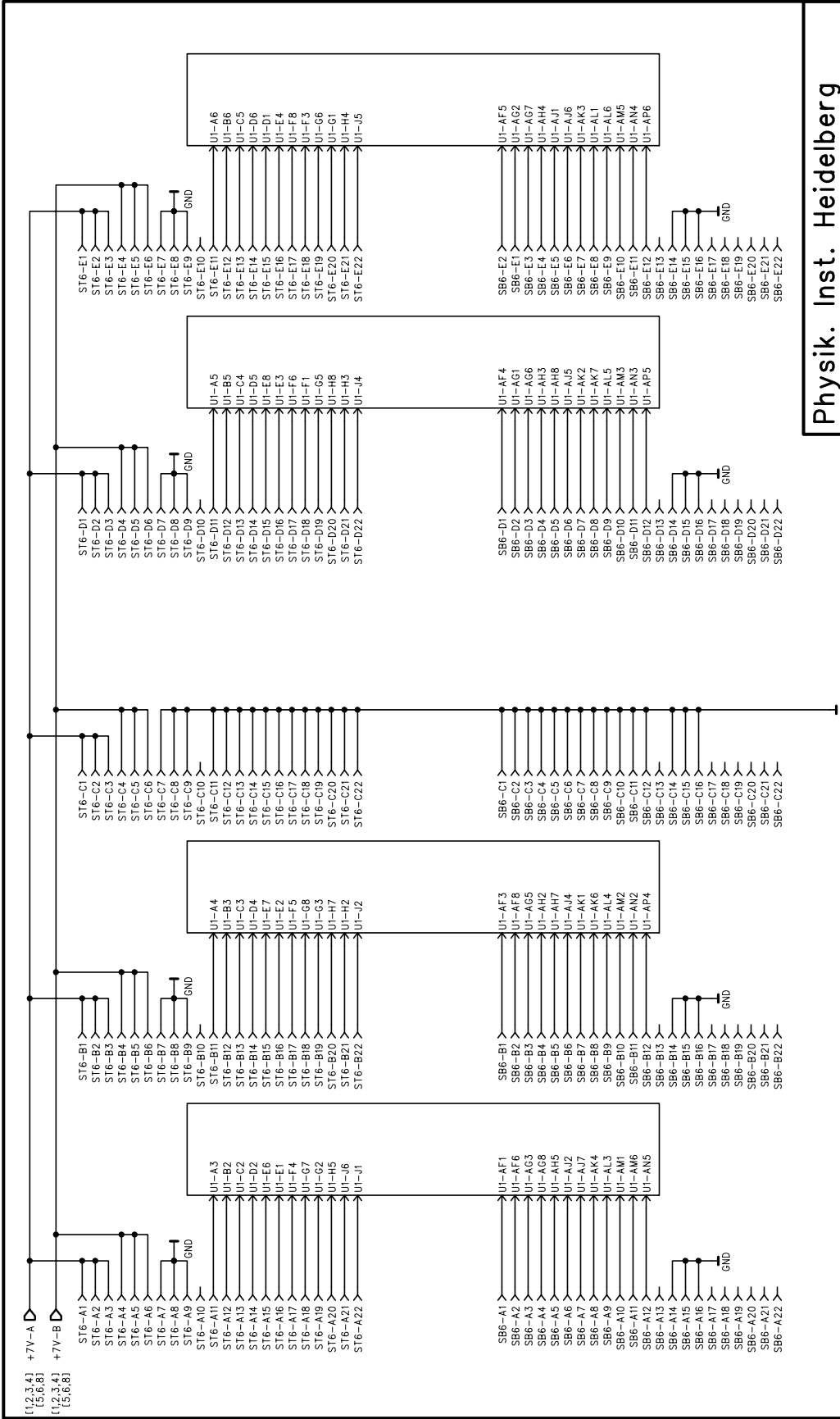
TOF-Logic-Backplane Control I/O/Slot5

Massstab: A4	Dat.: 1-uDEC-2006	Zeichn. Nr.: L167B-0	Bl.Nr.: 5 von 9
		Gez.: A. Rausch	

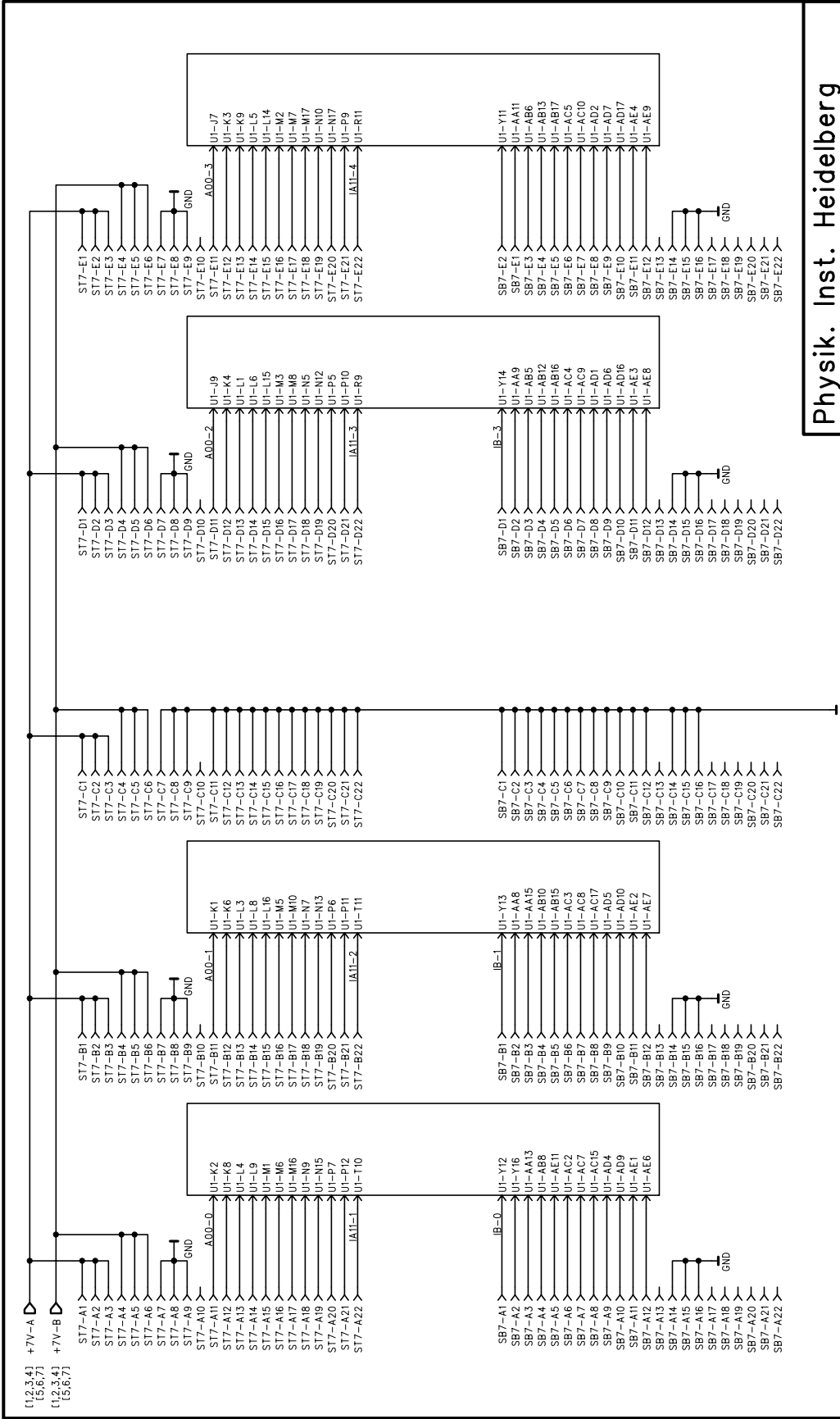


Physik. Inst. Heidelberg		TOF-Logic/Backplane IN4/Slot6	
		Massstab: A4	Zeichn. Nr.: L167B-0
Bl.Nr.: 6 von 9		Gez.: A. Rausch	

Dat.: 1-JUN-2006		Bl.Nr.: 6 von 9	
Gez.: A. Rausch		Zeichn. Nr.: L167B-0	



<b>Physik. Inst. Heidelberg</b> TOF-Logic/Backplane IN5/Slot7		Bl.Nr.: 7 von 9
		Zeichn. Nr.: <b>L167B-0</b>
Massstab: <b>A4</b>	Dat.: 1-JUN-2006	Gez.: <b>A. Rausch</b>



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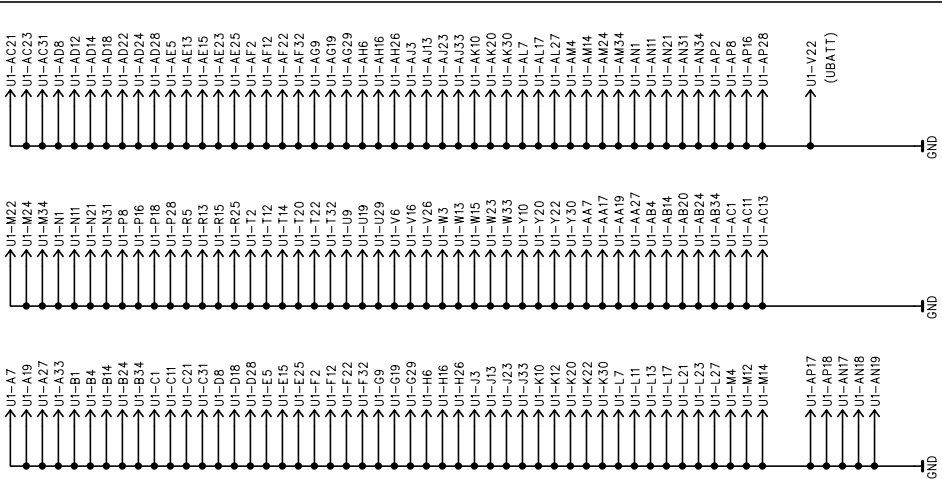
TOF-Logic/Backplane IN6/Slot8

<b>Massstab:</b> A4	<b>Dat.:</b> 1-JUN-2006	<b>Bl.Nr.:</b> 8 von 9
<b>Gez.:</b> A. Rausch		<b>Zeichn. Nr.:</b> L167B-0

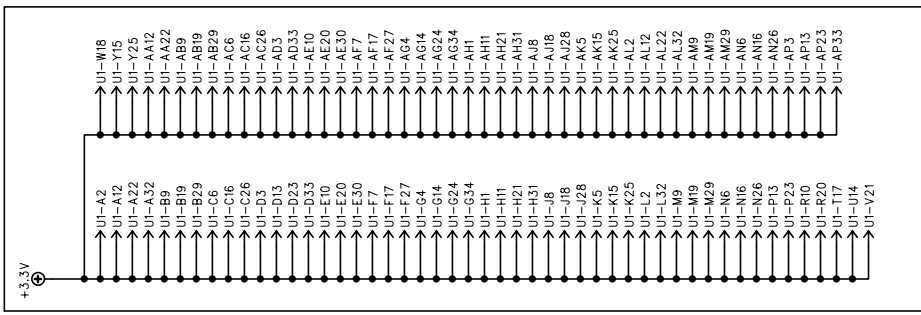


Power for Xilinx: LX40

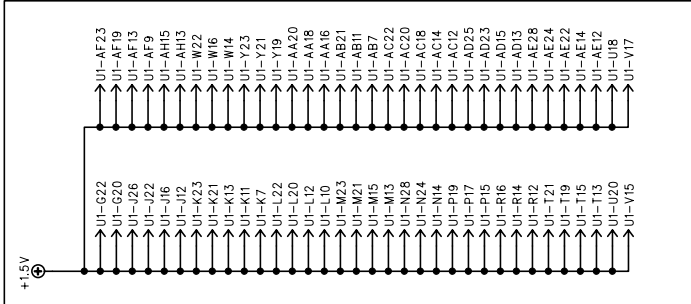
**GND**



**VCCO**

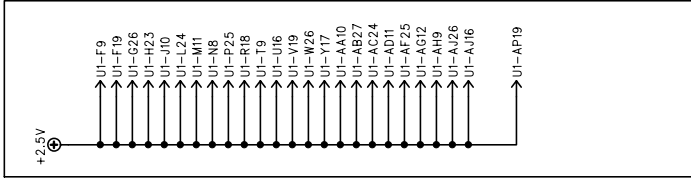


**VCCINT**

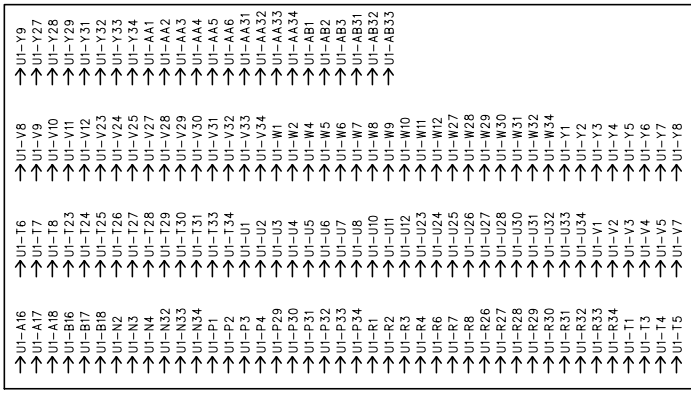


- Free I/O
- UI-J20
  - UI-K16
  - UI-K17
  - UI-K18
  - UI-K19
  - UI-AJ17
  - UI-AK8
  - UI-AK26
  - UI-AL26
- unused Dedicated
- TDP → UI-D15
  - TEN → UI-F15
  - D\_IN → UI-T16
  - PWRDWN\_LB → UI-W21

**VCCAUX**



**n (no Connected PINs)**



**Physik. Inst. Heidelberg**

**TOF-Logic/Backplane FPGA-Power**

Massstab: <b>A4</b>	Dat.: 1-JUN-2006	Zeichn. Nr.: <b>L167B-0</b>	Bl.Nr.: <b>9</b> von <b>9</b>
	Gez.: A. Rausch		